

CLAIMS

1. A decoder comprising a plurality of tuners for receiving data from different sources, each having an associated demultiplexer controlled to select
5 a portion of a received signal corresponding to a selected channel or channels, the demultiplexers being arranged to output to a remultiplexer configured to determine selected signal portions that have overlapping addresses, to reallocate addresses of the signal portions so there is no overlap, and to multiplex the signal portions for supply to a common interface slot.
- 10 2. A decoder according to Claim 1, in which the common interface slot is arranged to route the multiplexed signal portions through any inserted common interface card and then on to a demultiplexer for dividing the multiplexed signal portions and routing at least a part of the divided output to
15 its destination.
- 20 3. A decoder according to Claim 1, further comprising a switching unit connecting the demultiplexers to a number of remultiplexers, the switching unit being arranged to accept signal portions from the demultiplexers and to selectively switch each signal portion to one or more of the remultiplexers, each remultiplexer being configured to determine those signal portions that have overlapping addresses, to reallocate addresses of the signal portions so there is no overlap, and to multiplex the signal portions for supply to a common interface slot.
- 25 4. A decoder according to Claim 3, in which each remultiplexer is connected to a different common interface slot.
- 30 5. A decoder according to Claim 3, in which a signal portion is switched to a remultiplexer in dependence on its content.

6. A decoder according to Claim 3, in which a signal portion is switched to a remultiplexer in dependence on its source.
7. A decoder according to Claim 1, in which an address comprises a
5 channel identifier.
8. A decoder according to Claim 1, in which upon reallocating an address, a new index stream is created and embedded within the signal portion.

